AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

1. (currently amended): A semiconductor integrated circuit comprising:

a power supply wiring; ~~and~~

a ground wiring; and

a decoupling capacitor formed between said power supply wiring and said ground wiring, said decoupling capacitor having electrodes,

wherein at least one of the electrodes of said decoupling capacitor ~~consists of~~ comprises a shield layer formed in a plane shape on a semiconductor substrate, and said shield layer is connected electrically directly to the semiconductor substrate via a diffusion layer and is fixed to a power supply potential or the ground potential.

2. (currently amended): The semiconductor integrated circuit as claimed in claim 1, wherein, ~~out of~~another of the electrodes of said decoupling capacitor, ~~the electrode opposing~~ which opposes the electrode ~~consisting of~~comprising said shield layer, ~~consists of~~includes a wiring layer connected to wirings on ~~the~~an uppermost layer of a multilayer wiring structure via contact electrodes, and a capacitor insulating film for forming said decoupling capacitor is provided between said wiring layer and said shield layer.

3. (currently amended): A semiconductor integrated circuit comprising:

a power supply wiring; ~~and~~

a ground wiring; and

a decoupling circuit formed between said power supply wiring and said ground wiring, said decoupling circuit having electrodes,

wherein at least one electrode of said decoupling ~~capacitor consists of~~circuit comprises a shield layer obtained by covering a plurality of protrusions formed on a semiconductor substrate, and said shield layer is electrically connected directly to the semiconductor substrate via a diffusion layer and is fixed to a power supply potential or the ground potential.

4. (currently amended): The semiconductor integrated circuit as claimed in claim 3, wherein said protrusions are formed simultaneously with a gate electrode by ~~the identical~~a same formation process used for the gate electrode.

5. (currently amended): The semiconductor integrated circuit as claimed in claim 1~~ or 3~~, wherein said decoupling capacitor is formed on an element isolation oxide film.

6. (currently amended): The semiconductor integrated circuit as claimed in claim 1 ~~or 3~~, wherein said shield layer ~~consists of~~comprises a silicon compound of a metal.

7. (new): The semiconductor integrated circuit as claimed in claim 3, wherein said decoupling circuit is formed on an element isolation oxide film.

8. (new): The semiconductor integrated circuit as claimed in claim 3, wherein said shield layer comprises a silicon compound of a metal.

9. (new): The semiconductor integrated circuit as claimed in claim 1, wherein said diffusion layer is a well contact diffusion layer.

10. (new): The semiconductor integrated circuit as claimed in claim 3, wherein said diffusion layer is a well contact diffusion layer.

11. (new): The semiconductor integrated circuit as claimed in claim 1, wherein said semiconductor substrate includes a p-well region and a n-well region.

12. (new): The semiconductor integrated circuit as claimed in claim 3, wherein said semiconductor substrate includes a p-well region and a n-well region.